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11-22-00 A

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. TN201
Total Pages in this Submission

JC965 U.S. PTO 11/21/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

JC918 U.S. PTO 09/717963 11/21/00

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHODS AND APPARATUS FOR FACILITATING THE DESIGN OF AN ADAPTER CARD OF A COMPUTER SYSTEM

and invented by:

Daniel A. Jochym and Rama Rao V. Voddi

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____
Which is a:
☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____
Which is a:
☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

APPLICATION ELEMENTS

1. ☒ Filing Fee as calculated and transmitted as described below

2. ☒ Specification having 12 pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if applicable)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. TN201 Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☐ Formal Number of Sheets _____
   b. ☒ Informal Number of Sheets 2

4. ☒ Oath or Declaration
   a. ☐ New executed *(original or copy)* ☒ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional applications only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ DELETION OF INVENTOR(S)

      Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b)

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*

   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference herein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgement postcard
14. ☒ Certificate of Mailing

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UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. TN201 Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☐ Certified copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Additional Enclosures *(please identify below)*:

Associate Power of Attorney

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	**11**	**- 20 =**	**0**	**$18**	**$0.00**
Indep. Claims	**3**	**- 3 =**	**0**	**$80**	**$0.00**
Multiple Dependent Claims (check if applicable) ☐					**$0.00**
				BASIC FEE	**$710.00**
OTHER FEE *(specify purpose)* _____					**$0.00**
				TOTAL FILING FEE	**$710.00**

☐ A check in the amount of _____ to cover the filing fee is enclosed.

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- ☐ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: November 21, 2000

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): Daniel A. Jochym et al.			DOCKET NO. TN201
Serial No. **To Be Assigned**	Filing Date Herewith - 21 Nov. 2000	Examiner N/A	Group Art Unit N/A

Invention: METHODS AND APPARATUS FOR FACILITATING THE DESIGN OF AN ADAPTER CARD OF A COMPUTER SYSTEM

I hereby certify that this **utility patent application and indicated enclosures** is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on November 21, 2000.

Rocco L. Adornato

(Type or Printed Name of Person Mailing Correspondence)

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METHODS AND APPARATUS FOR FACILITATING THE DESIGN OF AN ADAPTER CARD OF A COMPUTER SYSTEM

FIELD OF THE INVENTION

This invention relates to apparatus and methods for designing adapter cards for computer systems.

BACKGROUND

Many types of adapter cards for computer systems, including high performance I/O cards, consist of two sections, an I/O interface section and a processor section. The I/O interface section usually implements an industry standard I/O interface, such as, for example, the Small Computer Systems Interface (SCSI), the Asynchronous Transfer Mode (ATM) interface, the Fibre Channel interface, the Universal Serial Bus interface, the IEEE 1394 interface, the Ethernet and other common network interfaces, and other well known I/O interfaces. The processor section typically adds intelligence to the adapter card and enables it to perform capabilities not usually found in adapter cards based solely on an industry standard interface. A typical processor section often comprises a processor, memory, control logic, and maintenance logic. These components may or may not also be industry standard or off-the-shelf components. The processor section typically executes proprietary program code that defines the added capabilities of the card. The software is usually stored within a non-volatile storage medium on the card, such as a read only memory (ROM) or the like.

Developing high performance computer I/O cards in today's swiftly changing marketplace is a challenging task, particularly where time to market is critical. Designing a high

performance adapter card having separate I/O and processor sections is particularly difficult because one section usually cannot be tested without the other section. Thus, for example, a delay in the design of the I/O section may hold up testing and debugging of the software and hardware of the processor section. Another difficulty in designing a high performance adapter card of this type is that the I/O sections are typically implemented using chipsets of other manufacturers. Delay in the planned release of a new chipset by one of these manufacturers may again hold up the design and testing of the processor section of a card. The dependence of the I/O and processor sections on each other also makes it difficult to test the processor section with different types of I/O interfaces and with chipsets from different manufacturers.

Consequently, a need exists for methods and apparatus that facilitate the design, testing, and debugging of high performance adapter cards having separate I/O and processor sections. The present invention satisfies this need.

SUMMARY OF THE INVENTION

The present invention enables the design and debug of both the I/O and processor sections of an adapter card to be coordinated. The invention allows a manufacturer to debug the processor module of an adapter card using a secondary PCI connector until the final design of the I/O module is completed. The present invention is embodied in the form of a printed circuit board adapted for prototyping. The present invention also encompasses a method of using the printed circuit board.

According to the present invention, a printed circuit board adapted for prototyping comprises a processor module, a section reserved for an I/O module to be added at a later time, a first and a second connector, a bridge circuit and a secondary bus. The processor module is

designed on a first portion of the printed circuit board and a second portion of the board is reserved for an input/output (I/O) module to be added at a later time. The first connector enables the card to be connected to a primary bus of a computer system. The bridge circuit bridges the primary bus of the computer system to a secondary bus on the printed circuit board. The secondary bus provides a communication path between the processor module and the I/O module that is to be added at a later time. The second connector is coupled to the secondary bus to enable a separate I/O card to be connected to the printed circuit board and to serve temporarily as the I/O module of the board. This permits prototyping in the absence of an I/O module in the second portion of the board.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing summary, as well as the following detailed description of the preferred embodiments, is better understood when read in conjunction with the attached drawings. For the purpose of illustrating the invention, there is shown in the drawings embodiments that are presently preferred, it being understood, however, that the invention is not limited to the specific apparatus, system, and instrumentalities disclosed. In the drawings:

FIG. 1 is a block diagram of an adapter card according to an embodiment of the present invention.

FIG. 2 is a flowchart that shows a method of making and prototyping an adapter card according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings wherein like numerals represent like elements throughout, there is shown in FIG. 1 a printed circuit board 5 adapted for prototyping. The printed circuit board 5 comprises a processor module 10, a first connector 15, a bridge circuit 20, a secondary bus 50 and a second connector 25. In the preferred embodiment, the first 15 and second 25 connectors, the secondary bus 50, and the bridge circuit 20 are implemented in accordance with the Peripheral Component Interconnect (PCI) architecture.

The processor module 10 is designed on a first portion 30 of the printed circuit board 5. The processor module 10 may perform a variety of functions, such as serving as a data router between an I/O module 40 and a computer system (not shown) in which the printed circuit board will be inserted. The processor module 10 may comprise a Field Programmable Gate Array (FPGA) that implements program code to be executed by the processor module 10. Alternatively, the processor module may be implemented by discrete components. For example, the processor module may comprise a microprocessor, such as the i960 processor available from Intel corporation, together associated memory and control circuitry. The processor module 10 can receive instructions in many ways, such as, for example, from a Read Only Memory (ROM) on the printed circuit board or from the main computer system or another intelligent system without departing from the principles of the present invention.

A second portion 35 of the board is reserved for an input/output (I/O) module 40 to be added at a later time. For example, the board designer may not have completed the design of, or settled on a particular chipset for the I/O module.

The first connector 15 provides connection of the board 5 to a primary bus 45 of a computer system (not shown). In the preferred embodiment, the primary bus 45 of the computer

system implements the PCI bus architecture. The bridge circuit 20 bridges the primary bus 45 of the computer system to a secondary bus 50 on the printed circuit board 5. The secondary bus 50 provides a communication path between the processor module 10 and the I/O module 40 that is to be added at a later time.

The second connector 25 is coupled to the secondary bus 50 to enable a separate I/O card 55 to be connected to the printed circuit board 5 and to serve temporarily as the I/O module of the board 5. The temporary I/O module 55 permits prototyping of the processor module 10 in the absence of a permanent I/O module 40 in the second portion 35 of the board.

In a preferred embodiment, the second connector 25 comprises a straddle mount connector disposed on an upper edge of the adapter card 5. Various connectors, such as, for example, right angle or surface mount connectors can be used to implement the second connector without departing from the principles of the present invention.

FIG. 2 is a flow diagram of a method of designing an adapter card in accordance with the present invention. The method allows the processor and the I/O sections of an adapter card to be tested separately.

First, in step 210, a bridge circuit in communication with a first connector of the adapter card is provided on the adapter card under design. The bridge circuit bridges the primary bus of the computer system to a secondary bus on the printed circuit board. The secondary bus is adapted to provide a communication path between the processor module and the I/O module.

Next, in step 220, a second connector in communication with the secondary PCI bus is provided on the adapter card to enable a separate I/O card to be connected to the adapter card and to serve temporarily as the I/O module of the card. The second connector and the secondary PCI

bus permit prototyping of the processor module in the absence of an I/O module in the second section of the adapter card under design.

At step 230, a separate I/O card is connected to the second connector and at step 240, the user then operates the adapter card being prototyped with the separate I/O card serving temporarily as the I/O module of the card to test the functionality of the card.

Furthermore, the adapter card, according to the present invention, can be used in another capacity. The secondary connector can be used to test various I/O modules to determine how each module affects the functionality of the adapter card. Different I/O modules can include chipsets from various vendors or an entire module. In this respect, various I/O modules or chipsets are connected to the secondary connector and tested to see which I/O module performs most effectively with the adapter card. When one particular I/O module has been selected as the most effective, that I/O module can be permanently implemented in the second section of the adapter card.

Referring again to FIG. 2, in step 250, the separate I/O module is removed from the second connector when testing of the functionality of the adapter card is completed. Then, in step 260, a permanent I/O module is implemented in the second section of the adapter card and the second connector may be removed from the design. The second connector, however, does not need to be removed from the design, it can, for example, be left in place as a debugging port or the like. The resulting design is then used to produce the final end product.

As the foregoing illustrates, the present invention is directed to an apparatus and methods for designing adapter cards for computer systems, including without limitation high performance computer input/output (I/O) cards. It is understood that changes may be made to the embodiments described above without departing from the broad inventive concepts thereof. For

example, the second connector may not be a straddle mount but a right angle or surface mount connector. Additionally, various components may not need to comply with PCI architecture. Therefore, the spirit and scope of the appended claims should not be limited to the description of the preferred embodiment contained herein.

WHAT IS CLAIMED IS:

1. A printed circuit board adapted for prototyping comprising:

a processor module designed on a first portion of the printed circuit board, a second portion of the board being reserved for an input/output (I/O) module to be added at a later time;

a first connector that provides connection of the board to a primary bus of a computer system;

a bridge circuit that bridges the primary bus of the computer system to a secondary bus on the printed circuit board, the secondary bus providing a communication path between the processor module and the I/O module that is to be added at a later time; and

a second connector coupled to the secondary bus to enable a separate I/O card to be connected to the printed circuit board and to serve temporarily as the I/O module of the board to permit prototyping of the processor module in the absence of an I/O module in said second portion of the board.

2. The printed circuit board of claim 1, wherein the processor module is intended to serve as a data router between the I/O module and the computer system.

3. The printed circuit board of claim 1, wherein said processor module comprises a Field Programmable Gate Array (FPGA) that implements program code to be executed by the processor module.

4. The printed circuit board of claim 1, wherein the primary bus of the computer system implements the Peripheral Component Interconnect (PCI) bus architecture, and wherein the first and second connectors, the secondary bus, and the bridge circuit are implemented in accordance with the PCI architecture.

5. The printed circuit board of claim 1, wherein said second connector comprises a straddle mount connector disposed on an upper edge of the card.

6. A method of prototyping an adapter card intended to have an I/O module in a second section of the card, a processor module in a first section of the card, and a first connector for connecting the adapter card to a primary bus of a computer system in which the card will be employed, the method comprising:

(a) providing on the adapter card being prototyped a bridge circuit in communication with the first connector of the adapter card to bridge the primary bus of the computer system to a secondary bus on the printed circuit board, the secondary bus adapted to provide a communication path between the processor module and the I/O module; and

(b) providing on the adapter card a second connector in communication with the secondary PCI bus to enable a separate I/O card to be connected to the adapter card and to serve temporarily as the I/O module of the card to permit prototyping of the processor module in the absence of an I/O module in the second section of the adapter card being prototyped;

(c) connecting a separate I/O card to said second connector; and

(d) operating the adapter card being prototyped with the separate I/O card serving temporarily as the I/O module of the card to test the functionality of the card.

7. The method recited in claim 6, further comprising the steps of:

(e) removing the separate I/O module from said second connector when testing of the functionality of the adapter card is completed; and

(f) implementing a permanent I/O module in the second section of the adapter card and removing the second connector from the card, the resulting adapter card comprising a production version of the card.

8. The method recited in claim 6, wherein steps (c) and (d) are repeated with other separate I/O cards to test the functionality of the adapter card with different I/O interface designs.

9. The method recited in claim 6, wherein the primary bus of the computer system implements the Peripheral Component Interconnect (PCI) bus architecture, and wherein the first and second connectors, the secondary bus, and the bridge circuit are implemented in accordance with the PCI architecture.

10. The method recited in claim 6, wherein said second connector comprises a straddle mount connector disposed on an upper edge of the card.

11. A method of prototyping an adapter card intended to have an I/O module in a second section of the card, a processor module in a first section of the card, and a first connector for connecting the adapter card to a primary bus of a computer system in which the card will be employed, the method comprising:

(a) providing on the adapter card being prototyped a bridge circuit in communication with the first connector of the adapter card to bridge the primary bus of the computer system to a secondary bus on the printed circuit board, the secondary bus adapted to provide a communication path between the processor module and the I/O module; and

(b) providing on the adapter card a second connector in communication with the secondary PCI bus to enable a separate I/O card to be connected to the adapter card and to serve temporarily as the I/O module of the card to permit prototyping of the processor module in the absence of an I/O module in the second section of the adapter card being prototyped;

(c) connecting a separate I/O card to said second connector; and

(d) operating the adapter card being prototyped with the separate I/O card serving temporarily as the I/O module of the card to test the functionality of the card; and

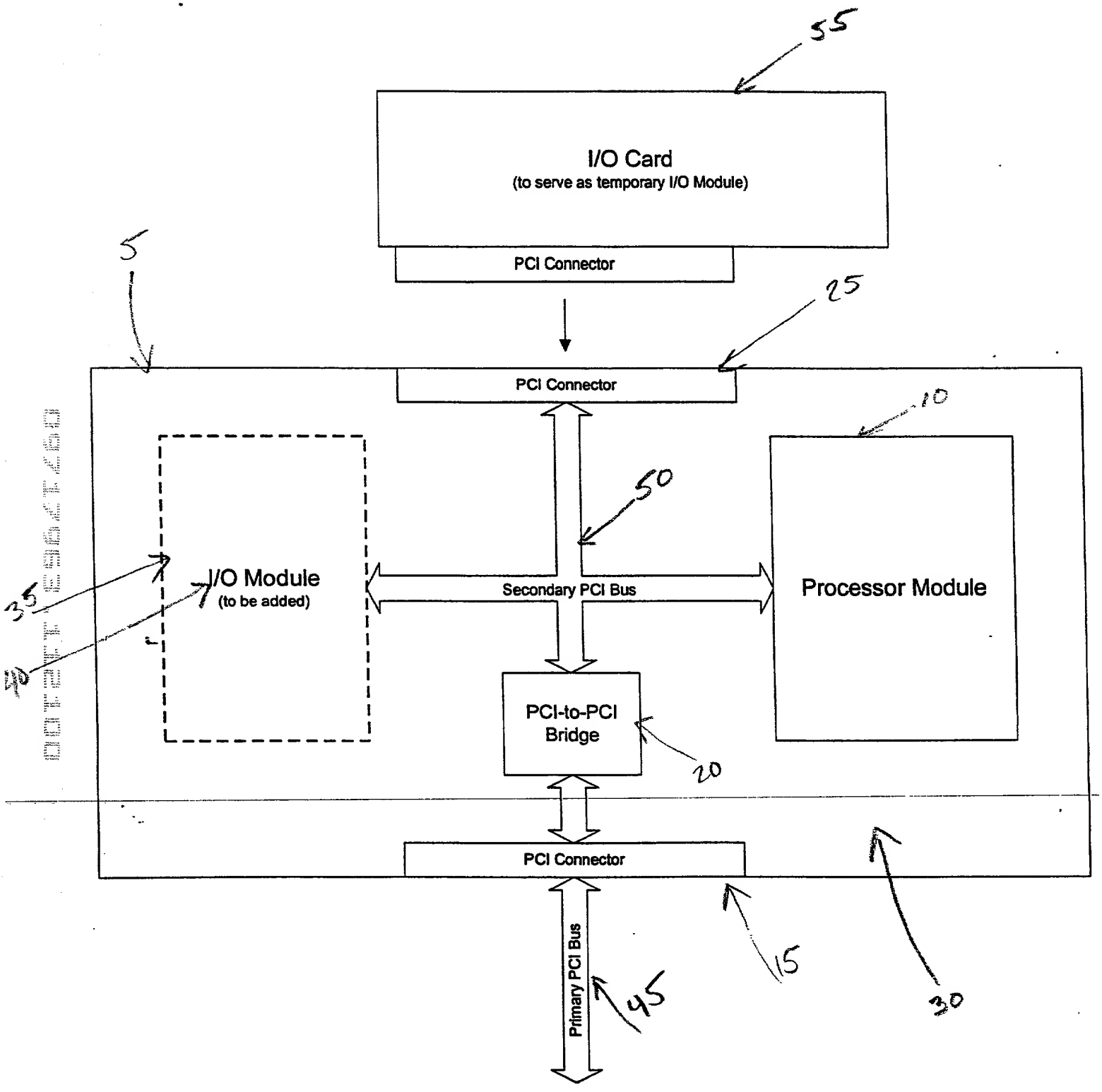
(e) repeating steps (c) and (d) with other separate I/O cards to test the functionality of the adapter card with different I/O interface designs; and

(f) determining which I/O interface design is preferred in the functionality of the adapter card; and

(g) implementing a permanent I/O interface in the second portion of the adapter card.

ABSTRACT

A printed circuit board adapted for prototyping comprises a processor module, a section reserved for an I/O module to be added at a later time, a first and a second connector, a bridge circuit and a secondary bus. The secondary bus provides a communication path between the processor module and the I/O module that is to be added at a later time. The second connector is coupled to the secondary bus to enable a separate I/O card to be connected to the printed circuit board and to serve temporarily as the I/O module of the board. This permits prototyping in the absence of an I/O module in the second portion of the board.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I/O Card
(to serve as temporary I/O Module)
PCI Connector
5
25
PCI Connector
10
50
I/O Module
(to be added)
35
Secondary PCI Bus
Processor Module
PCI-to-PCI
Bridge
20
PCI Connector
Primary PCI Bus
45
15
30

FIG. 1

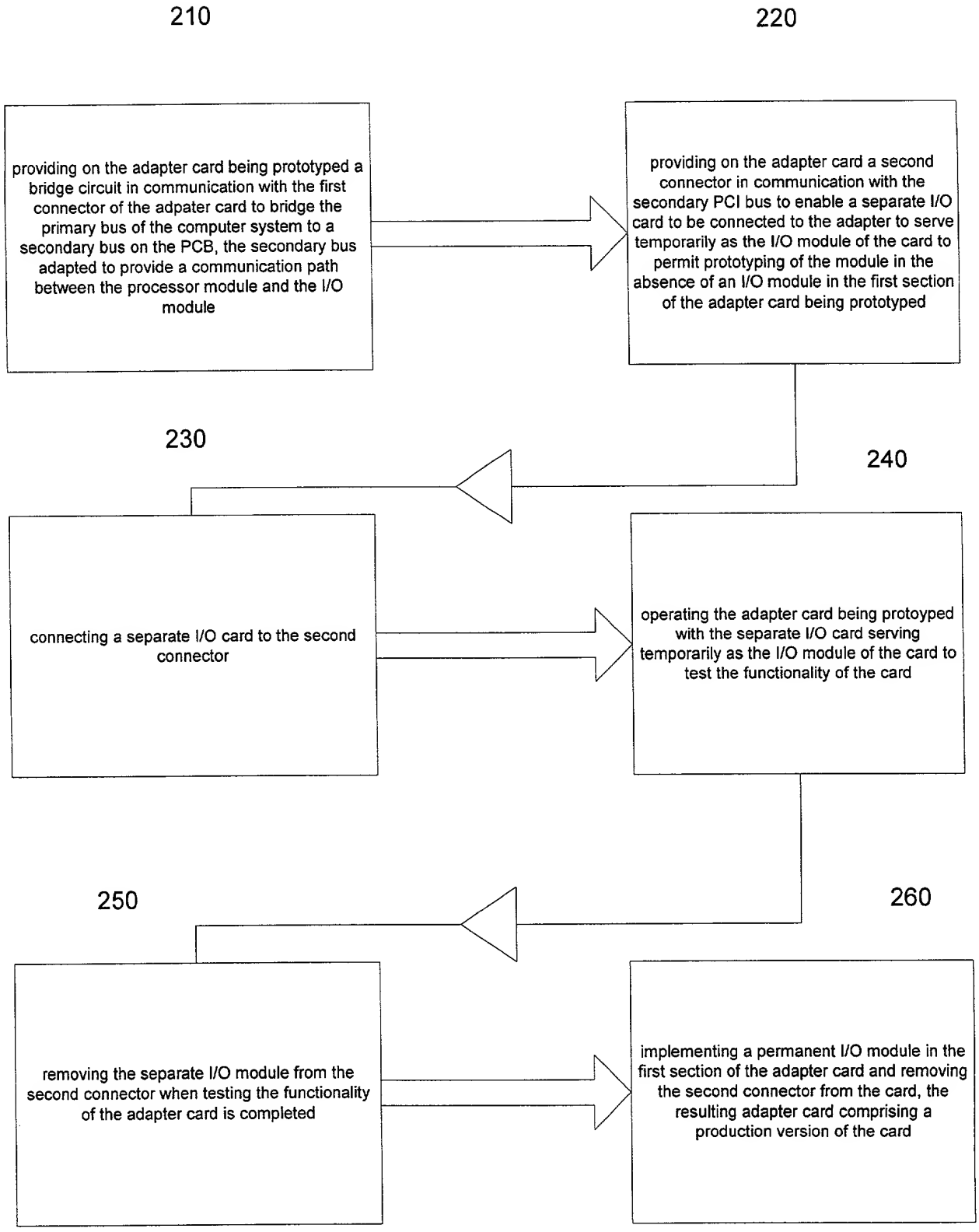
210
220
providing on the adapter card being prototyped a bridge circuit in communication with the first connector of the adpater card to bridge the primary bus of the computer system to a secondary bus on the PCB, the secondary bus adapted to provide a communication path between the processor module and the I/O module
providing on the adapter card a second connector in communication with the secondary PCI bus to enable a separate I/O card to be connected to the adapter to serve temporarily as the I/O module of the card to permit prototyping of the module in the absence of an I/O module in the first section of the adapter card being prototyped
230
240
connecting a separate I/O card to the second connector
operating the adapter card being protoyped with the separate I/O card serving temporarily as the I/O module of the card to test the functionality of the card
250
260
removing the separate I/O module from the second connector when testing the functionality of the adapter card is completed
implementing a permanent I/O module in the first section of the adapter card and removing the second connector from the card, the resulting adapter card comprising a production version of the card

FIG. 2

Docket No. TN201/USYS-0076 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Daniel A. Jochym et al.

Group Art Unit: N/A

Examiner: N/A

For: METHODS AND APPARATUS FOR FACILITATING THE DESIGN OF AN ADAPTER CARD OF A COMPUTER SYSTEM

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; and

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a

☒ Utility Patent ☐ Design Patent

is sought on the invention, whose title appears above, the specification of which:

☒ is attached hereto.
☐ was filed on _____ as Serial No. _____.
☐ said application having been amended on

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to be material to the patentability of this application in accordance with 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a-d) of any **foreign application(s)** for patent or inventor's certificate listed below and

have also identified below any foreign application for patent or inventor's certificate having a filing date before that of any application on which priority is claimed:

Priority Claimed (If X'd)	**Country**	**Serial Number**	**Date Filed**
☐	_____	_____	_____
☐	_____	_____	_____

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to be material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	**Date Filed**	**Patented/Pending/Abandoned**
_____	_____	_____
_____	_____	_____

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Serial Number	**Date Filed**
_____	_____
_____	_____

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Name: Rama Rao V. Voddi	______________________ **Signature** **Date of Signature:** ______________ **Citizenship:**
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City/State of Actual Residence: Chester Springs, Pennsylvania 19425	

DOCKET NO. TN-201/USYS-0076 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Daniel A. Jochym, RamaRao V. Voddi

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filed: Herewith

Examiner: Not Yet Assigned

For: METHODS AND APPARATUS FOR FACILITATING THE DESIGN OF AN ADAPTER CARD OF A COMPUTER SYSTEM

Assistant Commissioner for Patents
Washington DC 20231

Sir:

ASSOCIATE POWER OF ATTORNEY

The undersigned, of the firm WOODCOCK WASHBURN KURTZ MACKIEWICZ & NORRIS LLP, One Liberty Place - 46th Floor, Philadelphia, Pennsylvania 19103, Attorney and/or Agents for Applicant(s), hereby appoints the following:

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his/her associates with full power to prosecute the above-identified application and to transact all business in the Patent Office connected therewith and requests that correspondence continue to be directed to the firm of WOODCOCK WASHBURN KURTZ MACKIEWICZ & NORRIS LLP at the above address.

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